The Ithaca InterSystems
EPROM MEMORY BOARD

Edition 1.1

1.0 INTRODUCTION

The Ithaca InterSystems EPROM Memory board is a versatile microcomputer memory module designed for 8-bit or 16-bit S-100 bus systems. It provides up to 64 kbytes, or as little as 1 kbyte, of non-volatile EPROM storage in any S-100 system. There are two assembled versions of the EPROM Memory board. The EP64 accommodates any of the following EPROMs: 2508, 2758, 2516, 2716, 2532, and 2732. The EP16 accepts 2708 EPROMs and with hardware modification by the user, T.I. 2716 EPROMs. Modification of the EP 16 board is described in section 3.0.

EPROMs (Erasable, Programmable Read Only Memory) provide the systems designer and user with an essential link between large, complex, and largely disk-based operating systems, and the more industrial, turn-key application. Such applications have become increasingly common, as the advanced computing power and performance/cost ratio of the new 16-bit processor systems in the modular, low-cost S-100 bus format makes custom-tailored control applications of all kinds more attractive.

In such systems, disk facilities are often neither necessary or practical. Harsh environments, naive operators, and other factors make disk storage non-optimal. Programs for such a system can reside in ROM or PROMs, the latter providing an inexpensive and flexible facility for program changes when these are necessary. The EPROM Memory board implements the EPROM function in an elegant, flexible, and reliable package, at reasonable cost.

Software can readily be developed using sophisticated disk system support, assuming the availability of a compiler that produces output suitable for EPROM program storage. The Ithaca InterSystems Pascal/Z compiler is ideal for this purpose.

Once the software is debugged, transfer to EPROM can be accomplished with any of a variety of EPROM burning equipment available. The InterSystems EPROM Programmer is one such device.

Program size is not a constraint. The EPROM Memory board accepts many different EPROM types, up to the 2732 variety, a 4k by 8-bit device. Using 2732s, the EPROM Memory board can contain 64 kbytes of program (data memory in such a system would reside in the extended addressing space of the S-100 bus).

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The EPROM Memory board represents a powerful component in any system where reliable, permanent data storage is needed, be it the latest 16-bit industrial application, or a more traditional, 8-bit general-purpose system.

Like all Ithaca InterSystems products, the EPROM Memory board is thoroughly tested before shipment, and should provide years of trouble-free service. It is important, however, that the board be inspected upon receiving; and in any event, service may some day be needed. The HARDWARE MANUAL InterSystems Policies section contains information about these subjects.

This manual provides the information required to operate the EPROM Memory board in a S-100 Bus system. A description of the board, instructions for preparing the board for use in a system, a functional overview of the board operation, and the board parts list are provided.

1.1 PHYSICAL DESCRIPTION

The Ithaca InterSystems EPROM Memory board is a standard 5 by 10 inch (12.7 by 25.4 cm), S-100 bus, plug-in circuit board. The EP64 assembly provides a regulated +5 V for the EPROMs. The EP16 provides regulated +5 V, -5 V, and +12 V for the three voltage 2708 EPROMs.

1.2 BOARD FEATURES

The InterSystems EPROM Memory board provides the user with an adaptable framework for managing firmware in an S-100 microcomputer system. Two assembled versions of the board are available: the EP16, for 2708 EPROMs; and the EP64, that accommodates a variety of EPROM types. EPROM Memory board features include the following:

* 16 EPROM capacity; arranged as two banks of eight EPROMs.

* Each bank of the EP64 is independently configurable to accept either 2508, 2516, 2716, 2532, 2732, or 2758 EPROMs or compatible ROMs.

* Each bank is independently addressable to any bank-sized boundary in the 16 Mbyte memory space.

* The PHANTOM facility allows the board to overlap system memory.

* EPROMs may be accessed in pairs for 16-bit data transfer.

* EPROMs may be disabled in pairs.

* From 0 to 4 wait states are jumper selectable, allowing operation in 6 MHz systems.

* The EP64 board may be configured for either fast access time or low power consumption.

1.3 EP16 AND EP64

To allow for greater flexibility in application, the EPROM Memory board is available in two assembled versions: the EP16 and the EP64.

The EP16 is assembled to support only 2708-type EPROMs. The board is shipped with the required headers installed. The EP16 version of the board provides three regulated supply voltages: +5 V, -5 V, and +12 V. With the maximum of sixteen 2708 EPROMs installed, the EP16 provides 16 kbytes EPROM memory storage. With hardware modification the EP16 can support T.I. 2716 EPROMs. The modification procedure is located in section 3.0 of this manual.

The EP64 version supports a variety of single-voltage EPROMs. The board provides regulated +5 V. The board is user configured to accommodate the desired EPROMs.

1.4 PHANTOM*

The Memory boards support the PHANTOM* facility that allows the EPROM Memory board to overlap system memory. Whenever either bank of the Memory board is selected the Memory board drives PHANTOM* active, disabling any system memory board that decodes the PHANTOM* line. If the board is being used in a system that does not support PHANTOM* on line 67 of the S-100 bus, check that the EPROM Memory board does not overlap system memory.

2.0 BOARD SETUP

This section describes the EPROM Memory board and provides the information required to prepare the board for operation in an S-100 bus system.

The EPROM Memory board is easily configured to accommodate one or two of a variety of types of EPROMs, and to function in a variety of S-100 based systems. Preparing the board requires setting switches, configuring jumpers, and installing headers. The location of these components, SW1 through SW4, J1 through J3, and H1 through H6 is indicated in Figure 1.

Note that the Memory board is organized as two banks of EPROMs. Each bank is configured independently. Each bank can be configured to accept one type of EPROM. A single bank can not contain different EPROMs that are not pin compatible. The discussion of board setup is organized functionally. The user may wish to configure Bank 1 differently than Bank 2 at each functional step.

Note that the EP16 board EPROM banks can only accommodate 2708 EPROMs.

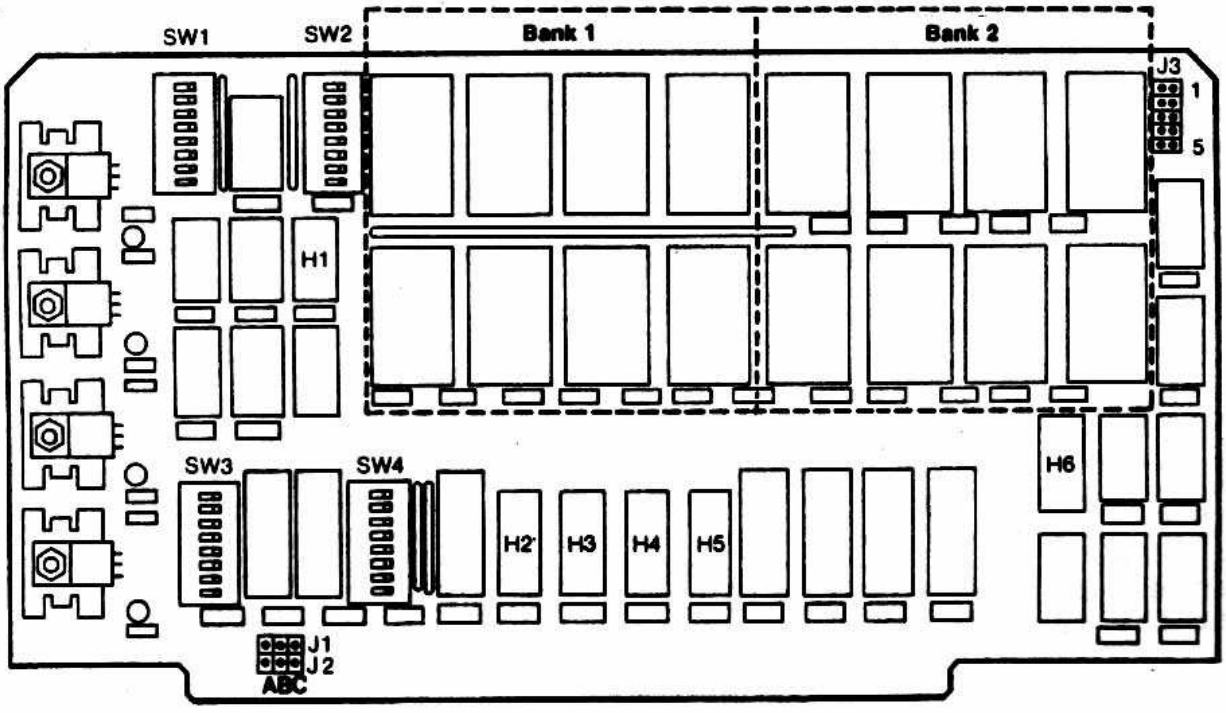


Figure 1 EPROM Memory board

2.1 JUMPER SUMMARY

Jumpers are used to configure the board to function in different S-100 bus systems. There are three jumper areas on the EPROM Memory board. Figure 1 shows the location of the jumpers. Each jumper area box contains a group of plated-through holes spaced 0.1" apart. To configure a jumper area, one connection per box is made between adjacent plated-through holes by a shunt that slides onto square posts that are soldered in the holes. Possible connections within jumper areas are designated by letter names. The letters run A, B, C, ... from left to right or from top to bottom. Jumpers J1 and J2 have three adjacent posts labeled A, B, and C. A shunt is used to connect either A to B, or B to C. Jumper 3 has five pairs of jumpers labelled A and B. One of the five possible positions is jumpered.

2.2 BANK BASE ADDRESS: SW1, SW2, SW3, SW4, J1, J2

The user may select the base address for each bank on any bank-sized boundary in system memory. Bank size is defined as the total memory size of eight EPROMs of the type specified for that bank. For example, if the bank is configured for 2716 EPROMs, then the bank is 16 kbytes and may be assigned any base address that follows: 000000H, 004000H, 008000H, ..., FFC000H. For a second example, if the bank is configured for 2732 EPROMs (4 kbytes), then the bank is 32 kbytes and may be assigned any base address that follows: 000000H, 0080000H, 010000H, ..., FF8000H.

Standard 16-bit addressing or extended 24-bit addressing is jumper selectable.

To avoid the conflict that would develop if the addresses of an enabled EPROM in Bank 1 overlap the address of an enabled EPROM in Bank 2, Bank 1 automatically disables Bank 2 when Bank 1 is accessed. Note that Bank 2 does not disable Bank 1 when Bank 2 is accessed. A conflict might occur if while Bank 2 is accessed, that Bank 1 is accessed in a shared memory space.

2.2.1 Bank 1

First, configure Bank 1 for either 16-bit or 24-bit addressing using jumper J1.

J1 A-B 24-bit addressing
J1 B-C 16-bit addressing

Next set switches SW1 and SW3 to configure the bank for the desired base address. See Figure 2 A switch set to the OPEN position decodes a logic ONE on the address line. Switches SW1-6 through SW1-8 correspond to address lines A13 through A15 respectively. If 24-bit extended addressing has been selected with J1, switches SW3-1 through SW3-8 correspond to address lines A23 through A16 respectively.

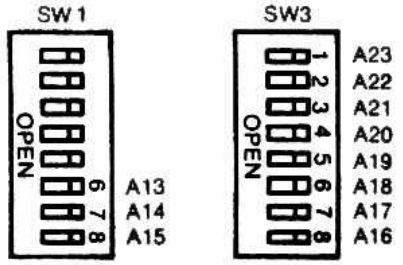


Figure 2 SW1 and SW3

2.2.2 Bank 2

First configure Bank 2 for either 16-bit or extended 24-bit memory addressing using J2.

J2 A-B 24-bit addressing
J2 B-C 16-bit addressing

Next set switches SW2 and SW4 to configure the bank base address as described above. See Figure 3. A switch set to the OPEN position decodes a logic ONE on the address line. Switches SW2-6 through SW2-8 correspond to address lines A13 through A15. If 24-bit extended addressing has been selected by J2, Switches SW4-1 through SW4-8 correspond to extended address lines A23 through A16 respectively.

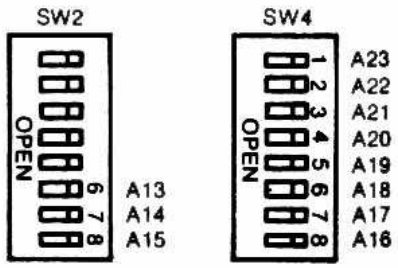


Figure 3 SW2 and SW4

2.3 ENABLING EPROM PAIRS: SW1 AND SW2

Each Memory board bank consists of four EPROM pairs. Each bank can be configured to support any combination of the four pairs. See Figure 4.

2.3.1 Bank 1

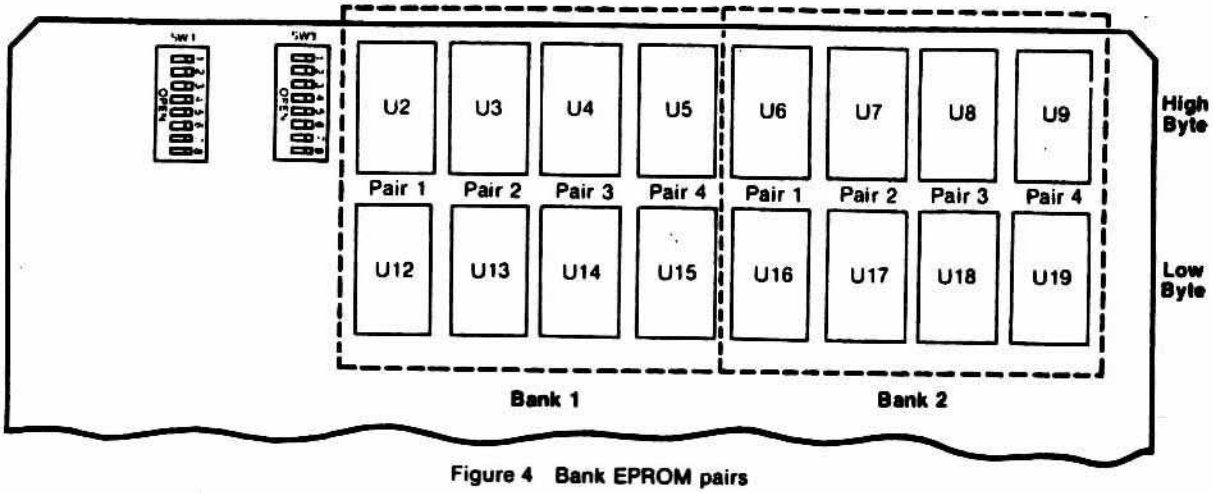


Figure 4 Bank EPROM pairs

The four EPROM pairs of Bank 1 are enabled/disabled by setting SW1 as shown in Figure 5. A switch set to the OPEN position disables the respective EPROM pair. A switch set to the CLOSED position enables the EPROM pair.

2.3.2 Bank 2

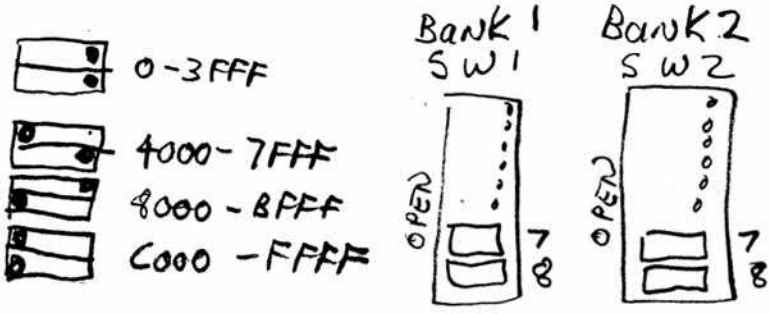
The four EPROM pairs of Bank 2 are enabled/disable by setting SW2 as shown in Figure 6. A switch set to the OPEN position disables the respective EPROM pair. A switch set to the CLOSED position enables the EPROM pair.

SW1-1	Pair 1	U2, U12
SW1-2	Pair 2	U3, U13
SW1-3	Pair 3	U4, U14
SW1-4	Pair 4	U5, U15

Figure 5 Bank 1 EPROM pair enable/disable

SW2-1	Pair 1	U6, U18
SW2-2	Pair 2	U7, U17
SW2-3	Pair 3	U8, U18
SW2-4	Pair 4	U9, U19

Figure 6 Bank 2 EPROM pair enable/disable



2.4 EPROM-TYPE CONFIGURATION

The EPROM Memory board has two EPROM banks. Each bank can be independently configured to accept one type of EPROM. A single bank can not contain different EPROMs that are not pin compatible.

NOTE: The EP16 board EPROM banks accommodates only 2708 EPROMs.

2.4.1 EPROM Type: H4 and H5

On the EP64 version of the board, each bank is configured to accept an EPROM type with a 16-pin DIP header. Header H4 is used to configure Bank 1. Header H5 is used to configure Bank 2. On the EP64 board, six different EPROMs are supported by four different headers, H4/5-1 through H4/5-5. Since both banks will often be configured to accommodate the same EPROM type, two each of the four different headers are required to support the six EPROM types. EP16 boards are shipped with the correct headers, H4/5-0, installed. See Figure 7.

Header	EPROM Type	Part #	Note Standard/Optional
H4/5-0	2708 (EP16)	1752	Standard on EP16
H4/5-1	2508, 2758	1755	Optional for EP64
H4/5-2	2516, 2716	1756	Standard on EP 64
H4/5-3	2532	1775	Optional for EP64
H4/5-4	2732	1759	Standard on EP64

Figure 7 H4 and H5

2.4.2 T.I. 2532 EPROMS/Fast Access/Low Power: H1 and H6

H1 is used to configure Bank 1; H6 is used to configure Bank 2. Three different headers are available for H1 and H6. See Figure 8.

Headers H1/6-1 are provided (in addition to headers H4/5-3) to configure the EP64 Memory board to accommodate Texas Instruments T.I. 2532 EPROMs.

For all EPROM types other than the T.I. 2532, the user can configure each bank of the EP64 to support either the "fast access" or "low power consumption" mode.

Header H1/6-2 configures the respective bank for low power consumption (up to 75% less power). This configuration might be advantageous if the Memory board is used to capacity.

Header H1/6-0 configures the respective bank of the EP64 for fast access mode (up to 75% faster).

The EP16 version of the board is shipped with H1/6-0 installed.

Header	Application	Part #	Note Standard/Optional
H1/6-0	EP16 board	1753	Standard on EP16
H1/6-0	Fast Access	1753	Standard on EP64
H1/6-1	T.I. 2532	1758	Optional for EP64
H1/6-2	Low power	1760	Optional for EP64

Figure 8 H1 and H6

2.5 8-BIT OR 16-BIT TRANSFERS: H2 and H3

The Memory board can be user-configured for either 8-bit (byte) data transfers or 16-bit (word) data transfers. When configured to operate in an 8-bit system, the board will provide 8-bit data from consecutive locations of a single EPROM, EPROM after EPROM, within the addressed bank.

When configured for 16-bit systems, the board will provide 16-bit data from EPROM pairs.

If the EPROM Memory board is configured for 8-bit operation and the system attempts a 16-bit read from the board (i.e., SXNTRQ*, line 58, active), the board will respond with data from the low EPROM of the enabled EPROM pair.

If the EPROM Memory board is configured for 16-bit operation and the system attempts an 8-bit read from the board (SXNTRQ* not active), The board will output either the even or the odd byte of the 16-bit word, depending on address line A0. The board is hardware configured to output the even byte when A0 is a logic ZERO, and the odd byte when A0 is a logic ONE.

Headers H2 and H3 are used to configure the board for either 8-bit or 16-bit operation. Note that each header has a notch indicating Pin 1. To install H2 and H3 for 8-bit addressing, install the header so that the notch corresponds to Pin 1 of the header socket - the upper-left corner. To install H2 and H3 for 16-bit addressing, install the header so that the notch corresponds to Pin 9 of the header - the lower-right corner. Both H2 and H3 must be installed the same way. Refer to Figure 9 to install H2 and H3.

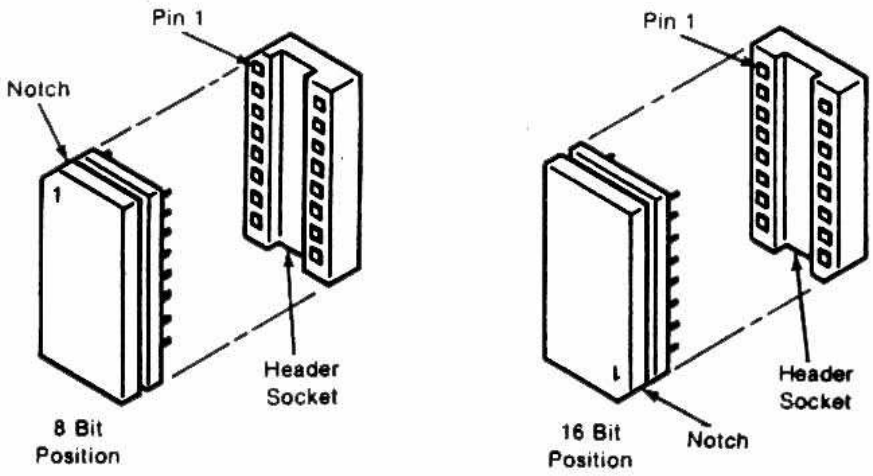


Figure 9 H2 and H3 installation

2.6 WAIT STATES

The EPROM Memory board can be configured to generate 0, 1, 2, 3, or 4 wait states when either bank is selected.

J3-1	4 Wait States
J3-2	3 Wait States
J3-3	2 Wait States
J3-4	1 Wait State
J3-5	0 Wait States

2.7 INSTALLING EPROMS

EPROMs are inserted with pin 1 oriented to the top left of the board as shown in Figure 10.

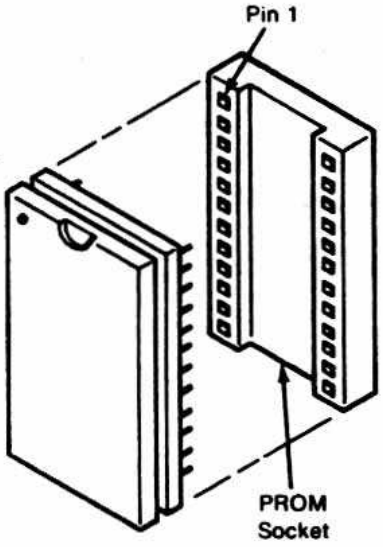


Figure 10 EPROM insertion

3.0 OPTIONS

This section provides information about the optional use of the EP16 board and optional headers for the EP64 board.

3.1 MODIFYING THE EP16 FOR T.I. 2716 EPROMS

The EP16 board can be adapted to read Texas Instrument T.I. 2716 EPROMs. The following cuts and jumpers can be made to modify Bank 1. For Bank 2 substitute H6 for H1, U34 for U24, U6-U9 and U12-U15 for U2-U5 and U12-U15, and SW2 for SW1 in the modification instructions. Once a bank (or both banks) has been modified to accept T.I 2716 EPROMs it must be re-modified to support 2708s again.

1) Remove header H1.

2) Cut U24p4-7 form SW1p1-4.

3) Cut U2-U5 and U12-U15 p20 from SW1p13-16.

4) Connect U24p9-12 to SW1p1-4.

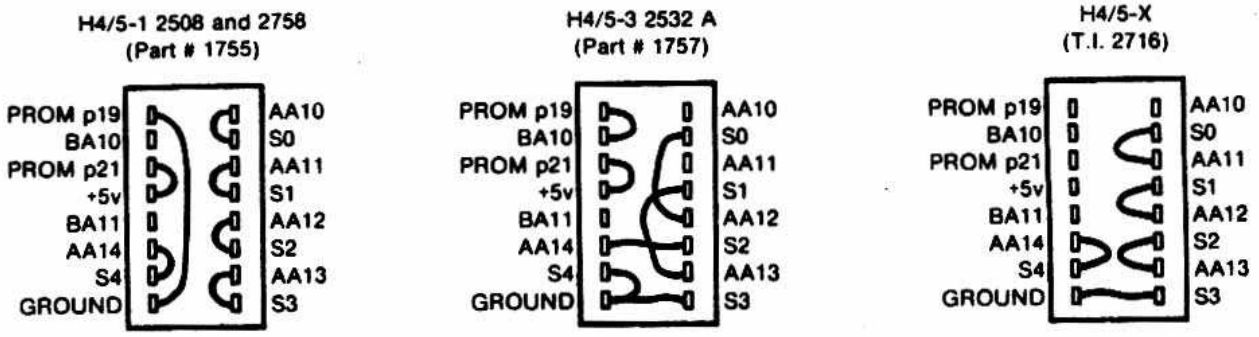
5) Connect U2-U5 and U12-U15p18 to SW1p13-16.

6) Connect U2-U5 and U12-U15p20 to BA10.

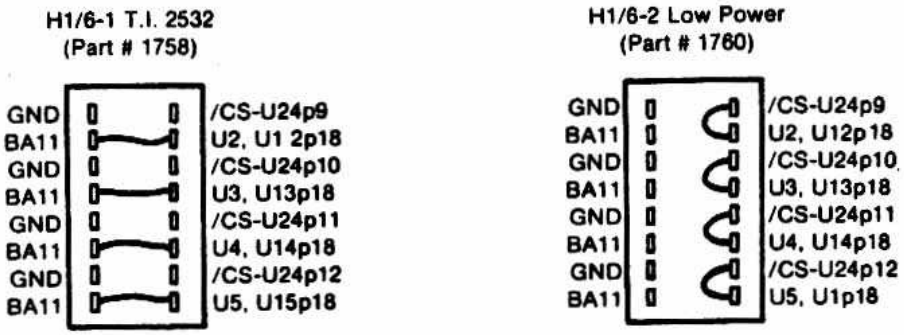
A new header, H4/5-X, must be made for H4/5. Instructions are located below.

3.2 HEADERS

The four optional headers not supplied with the board can either be purchased from InterSystems or built by the user. The following drawings illustrate the correct configuration of headers not supplied.



Optional H4/5 Headers



Optional H1/H6 Headers

Figure 11 Optional Headers

4.0 PARTS LIST

4.1 EP16 CARD

INTEGRATED CIRCUITS

U1	74LS20	U25,26	25LS2521
U10,11	74LS85	U27-31	74LS244
U20	74LS132	U32	74LS03
U21	74ALS74	U33	74LS175
U22	74LS00	U34	74LS155
U23	74LS04	U35	74LS14
U24	74LS155	U36	74LS158

RESISTORS

UR1-6	4.7 K OHM 9P SIP

CAPACITORS

C1-4,6-22,24-40,42-45,47-85	0.1 uf, AVX#MDO15E104Z
C5,23,41,46	10 uf, 35V

REGULATORS

Q1,4	7805
Q2	7905
Q3	7812

HEADERS

Standard, 2 each

H4/5-0	Part # 1752
H1/6-0	Part # 1753
H2/3	Part # 1742

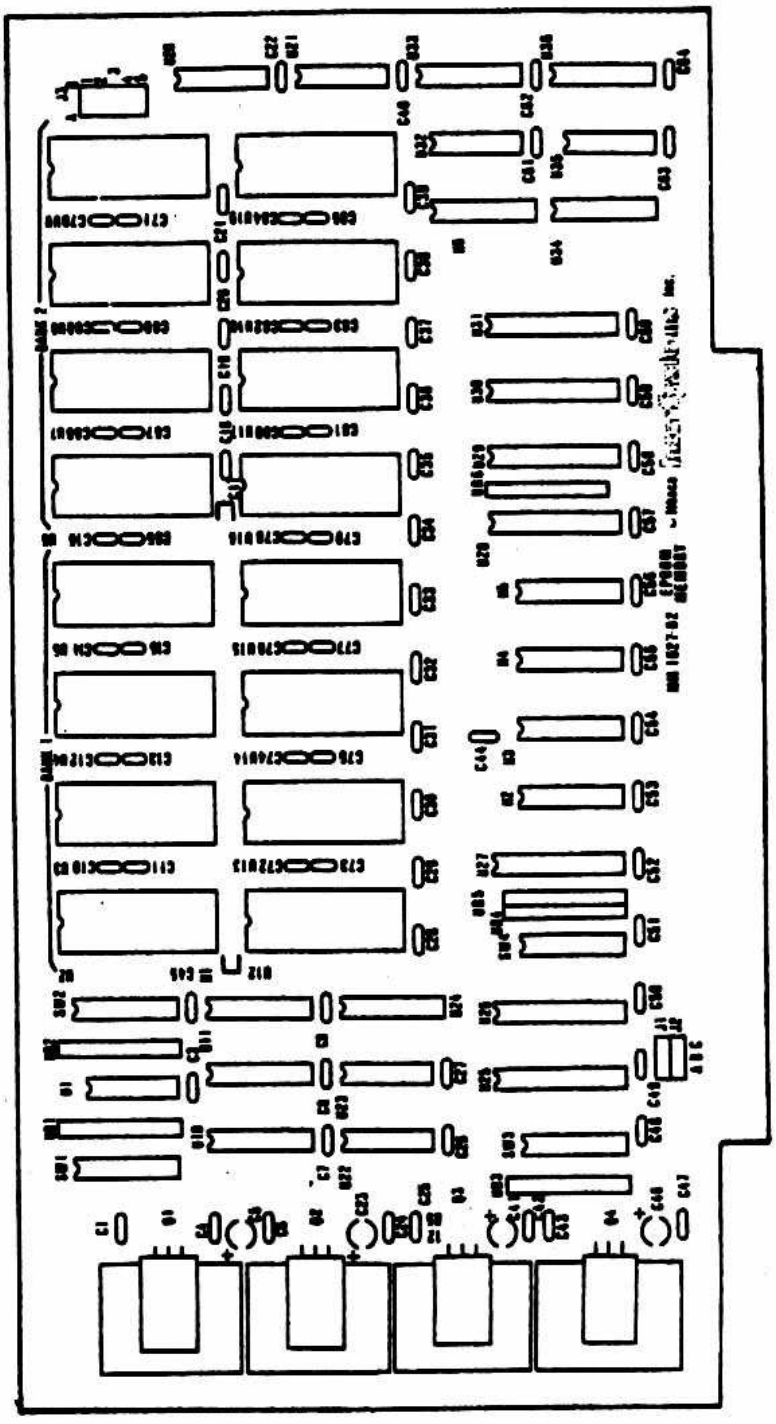


Figure 12

4.2 EP64 CARD

INTEGRATED CIRCUITS

U1	74LS20	U25,26	25LS2521
U10,11	74LS85	U27-31	74LS244
U20	74LS132	U32	74LS03
U21	74ALS74	U33	74LS175
U22	74LS00	U34	74LS155
U23	74LS04	U35	74LS14
U24	74LS155	U36	74LS158

RESISTORS

UR1-6	4.7 K OHM 9P SIP

CAPACITORS

C1-4,7-22,25-40,43-45,47-64	0.1 uf, AVX#MDO15E104Z
C46	10 uf, 35V

REGULATORS

Q1,3,4	7805

HEADERS

Standard, 2 each

H4/5-2	2516, 2716	Part # 1756
H4/5-4	2732	Part # 1759
H1/6-0	Fast Access	Part # 1753
H2/3	8-bit/16-bit	Part # 1754

Optional

H4/5-1	2508, 2758	Part # 1755
H4/5-3	2532	Part # 1757
H1/6-1	T.I. 2532	Part # 1758
H1/6-2	Low Power	Part # 1760

Change #: 1645-01-01 Page 1 of 2

Date: 11 JUNE 82

Board Name: EP16/64 (EPROM II)

Board Number: 1627

Problem Occurs in Revision: 01

Requested by: M WILLIAMS

APPROVAL

Approved:

To be included in PC @ Revision:

Date:

What is Change? (Please give brief summary)

TO MAKE BOARD ENABLE MEET IEEE S100 SPEC

Priority -- check one or more; each item must be individually approved. APR'D

---Update next PC. _____

---Include in new production. _____

---Include in all inventory (rework). _____

---Issue field update to customers. _____

Other: _____

(PLEASE use additional pages if required--it is not necessary to use this form for additional pages)

PROBLEM (describe clearly and legibly):

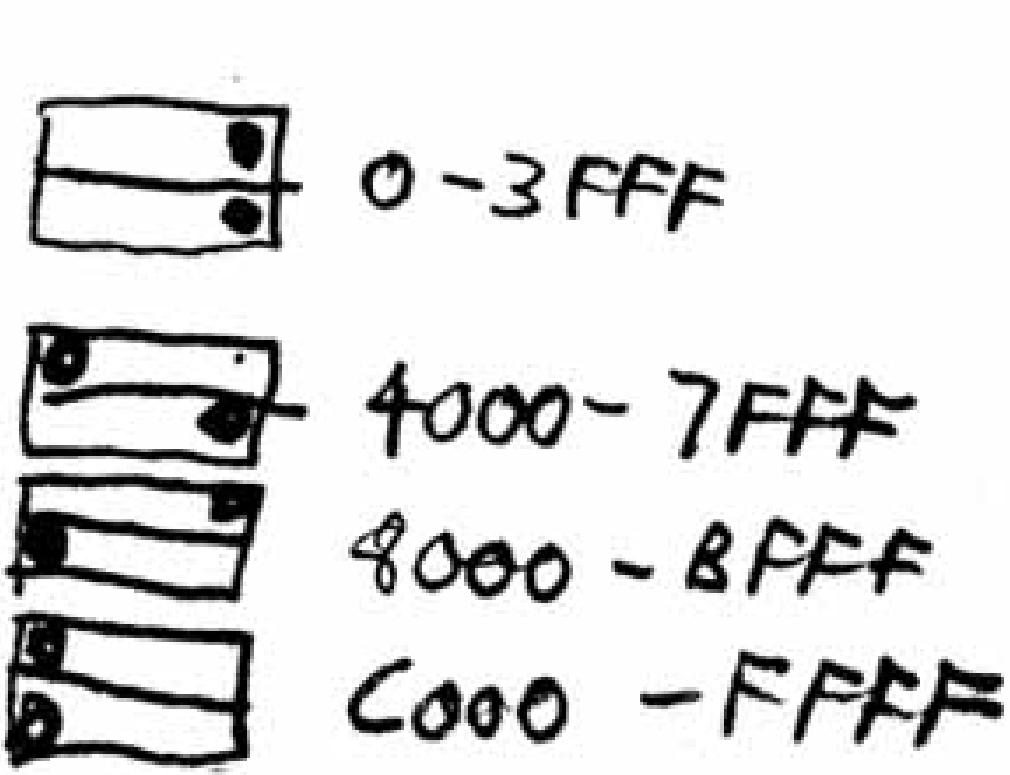
A FALSE BOARD ENABLE IS POSSIBLE UNDER IEEE S100 STANDARDS.

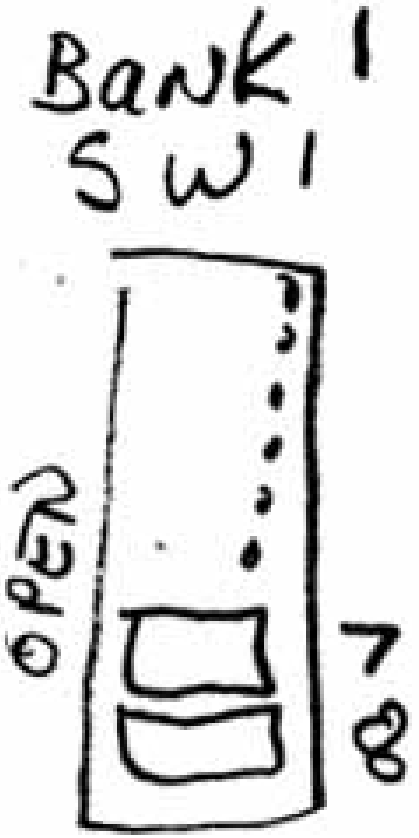
PROPOSED SOLUTION (describe clearly and legibly):

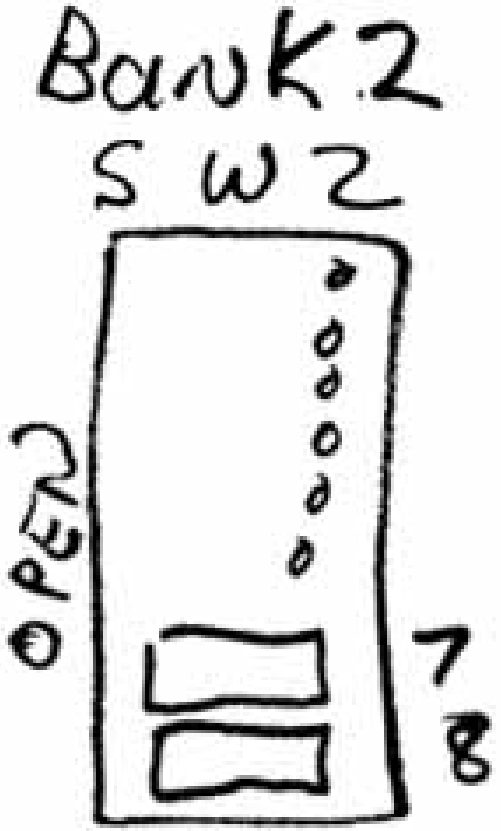
ENABLE BOARD ONLY ON NEGATIVE GOING EDGE OF $\overline{pSTVAC}$ DURING PSYNC HIGH.

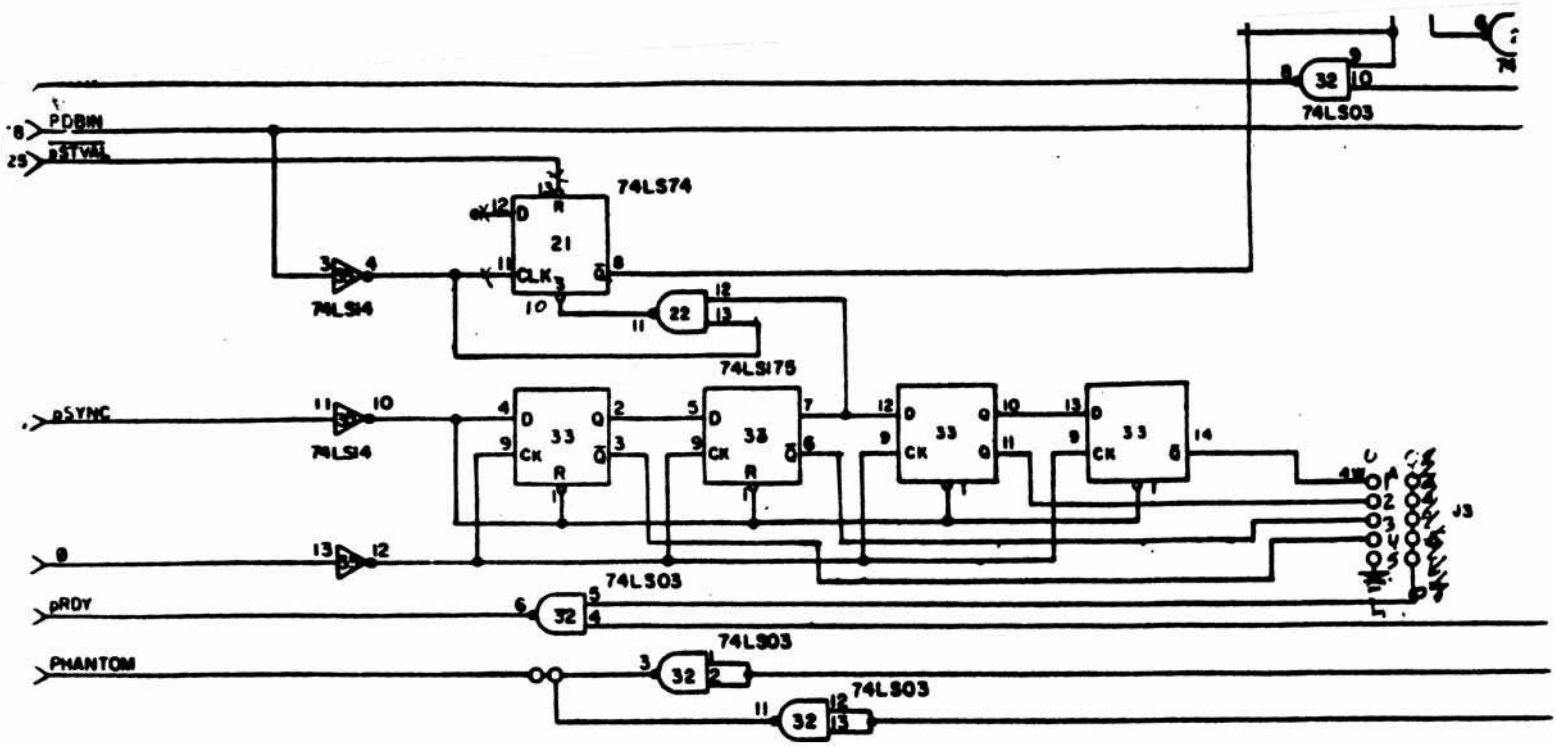
PROCEDURE (be specific, detailed, and legible; cuts and jumpers must include exact locations on PC board; future PC changes should be described separately from modifications of current product; parts changes should specify position, old part, and new part):

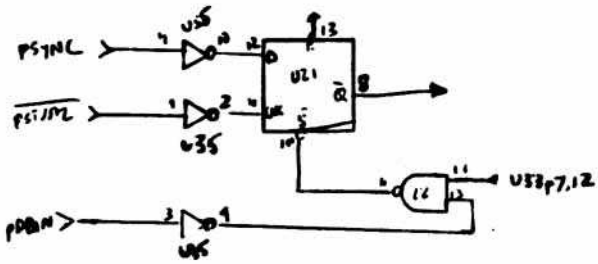
PLEASE SEE NEXT PAGE.


0-3FFF
4000-7FFF
8000-BFFF
C000-FFFF


Bank 1
SW1
OPEN
1
8


Bank 2
SW2
OPEN
1
8





① CUT U35p4 AND U22p13 FROM U21p11

② CUT PSTVAL FROM U21p13

③ CUT U21p12 FROM +5V (CUT PATH TRACES TO U21p12 AND JUMPER U21p TO +5V)

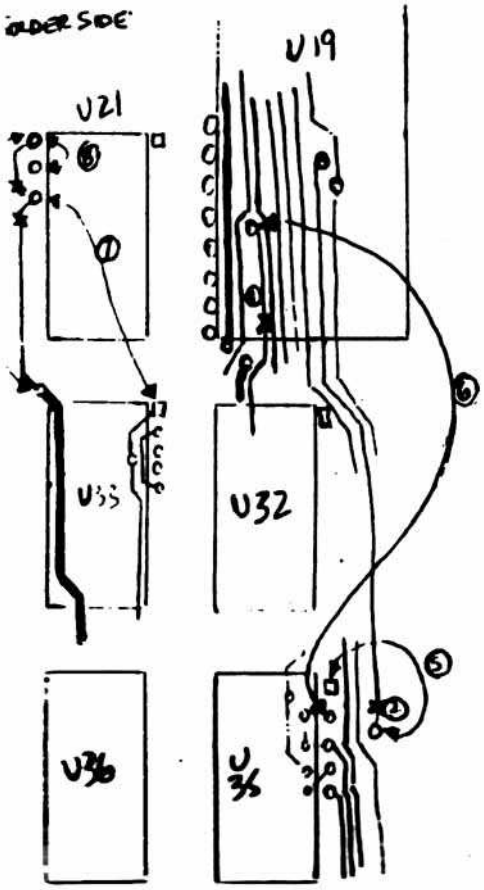
④ CUT U35p1 FROM +5V (U35p1,2 IS AN UNUSED GATE)

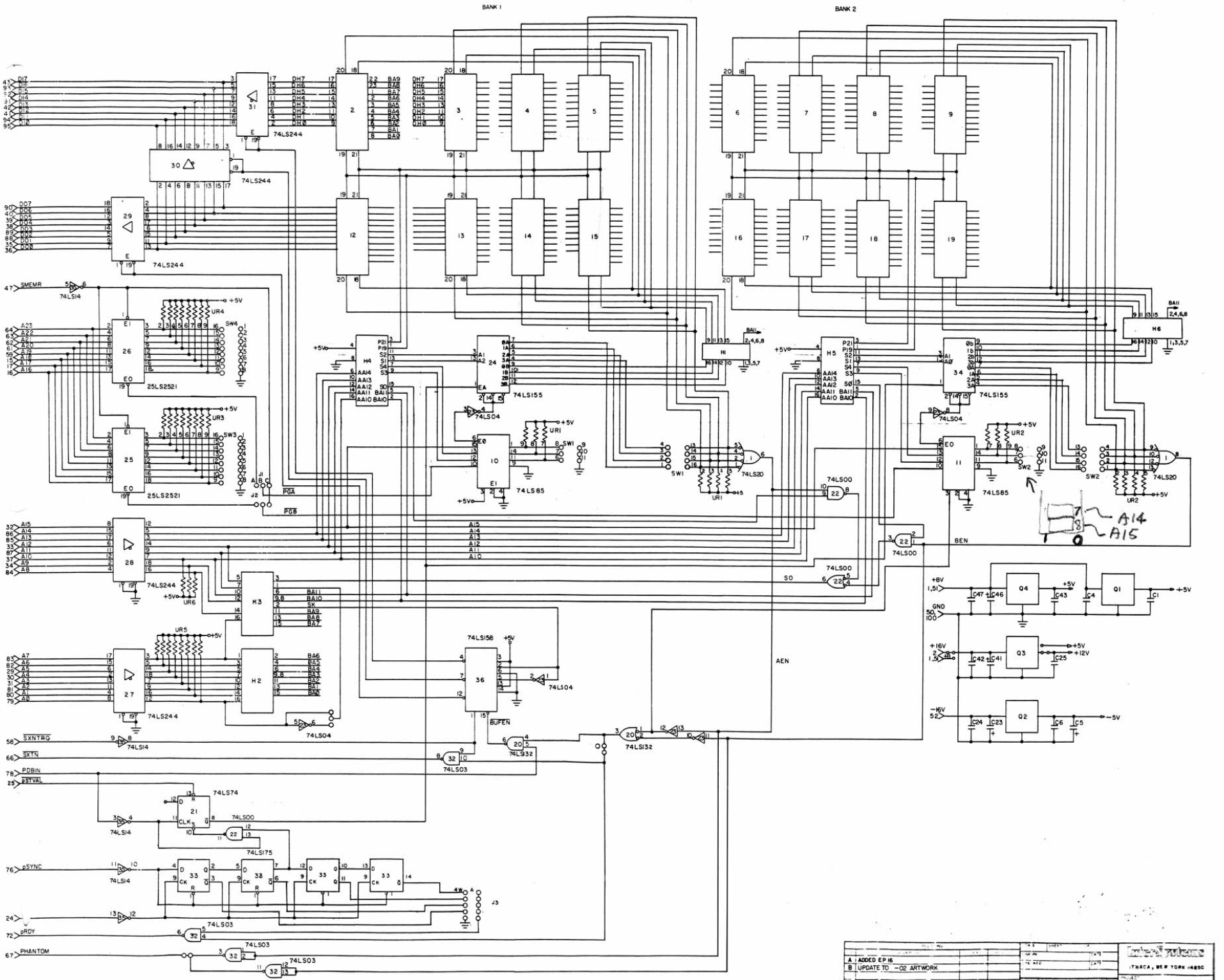
⑤ JUMPER PSTVAL TO U35p1

⑥ JUMPER U35p2 TO U21p11

⑦ JUMPER U35p10 TO U21p12

⑧ JUMPER U21p13 TO +5V




BANK 1
BANK 2
74LS244
74LS2521
74LS155
74LS85
74LS20
74LS00
74LS04
74LS14
74LS158
74LS32
74LS03
74LS74
74LS175
SMEMR
SXNTRQ
SXTN
PDBIN
PSTVAL
PSYNC
PRDY
PHANTOM
PGA
PGB
BUFEN
AEN
BEN
SO
A14
A15
+5V
+8V
+16V
-16V
GND
EPROM MEMORY
A : ADDED EP16
B : UPDATE TO -02 ARTWORK
UNLESS OTHERWISE NOTED
ITHACA, NEW YORK 14850
10-81
1828